CLAIMS

What is claimed is:

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1. A semiconductor device having a N-gate/N-substrate capacitor for characterizing polysilicon gate depletion corresponding to the semiconductor device, comprising:

an N doped substrate;

a gate oxide layer disposed over the N doped substrate;

a first isolation oxide and a second isolation oxide disposed over the N doped substrate and on opposing edges of the gate oxide layer;

an N+ doped gate disposed over at least one portion the first isolation oxide, the gate oxide, and the second isolation oxide.

2. The semiconductor device of Claim 1, wherein the gate is in a depletion mode simultaneously while the N doped substrate is in an accumulation mode.

3. The semiconductor device of Claim 1, wherein the polysilicon gate depletion of the semiconductor device corresponds to capacitor-voltage characteristics of the N-gate/N-substrate capacitor.

4. A semiconductor device having a P-gate/P-substrate capacitor for characterizing polysilicon gate depletion corresponding to the semiconductor device, comprising:

a P doped substrate;

a gate oxide layer disposed over the N-type substrate;

a first isolation oxide and a second isolation oxide disposed over the N-type substrate;

an P+ doped gate disposed over at least one portion of the first isolation oxide, the gate oxide, and the second isolation oxide.

5. The semiconductor device of Claim 4, wherein the gate is in a depletion mode simultaneously while the substrate is in an accumulation mode.

6. The semiconductor device of Claim 4, wherein the polysilicon gate depletion of the semiconductor device corresponds to capacitor-voltage characteristics of the P-gate/P-substrate capacitor.

7. A semiconductor capacitor structure, comprising:

an N doped substrate;

a gate oxide layer disposed over the substrate;

a first isolation oxide and a second isolation oxide disposed over the substrate;

an N+ doped gate disposed over the first isolation oxide, the gate oxide, and the second isolation oxide, wherein the semiconductor capacitor structure is used to characterize polysilicon gate depletion corresponding to a semiconductor fabrication process.

8. The semiconductor capacitor of Claim 7, wherein the gate is in a depletion mode while the substrate is in an accumulation mode.

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9. The semiconductor capacitor of Claim 7, wherein the polysilicon gate depletion corresponding to the semiconductor fabrication process is characterized by capacitor-voltage characteristics of the semiconductor capacitor.

10. A semiconductor capacitor structure, comprising:

an P doped substrate;

a gate oxide layer disposed over the substrate;

a first isolation oxide and a second isolation oxide disposed over the substrate;

an N+ doped gate disposed over the first isolation oxide, the gate oxide, and the second isolation oxide, wherein the semiconductor capacitor structure is used to characterize polysilicon gate depletion corresponding to a semiconductor fabrication process.

11. The semiconductor device of Claim 10, wherein the gate is driven into depletion while the substrate is simultaneously driven into accumulation.

12. The semiconductor device of Claim 10, wherein capacitance-voltage measurements are taken to characterize the polysilicon gate depletion of the semiconductor device.

13. A method for forming a P-gate/P-substrate capacitor for characterizing polysilicon gate depletion effect corresponding to a semiconductor fabrication process, comprising the steps of:

forming a silicon substrate;

growing an oxide layer over the silicon substrate;

etching the oxide layer to define a first isolation oxide section and a second oxide section;

growing a gate oxide disposed between the first isolation oxide section and the second isolation section;

depositing a polysilicon gate layer over the gate oxide;

defining the polysilicon gate;

doping the substrate with N dopants;

doping the polysilicon gate with N+ dopants;

laying and defining a metal layer.

14. The method of Claim 13, wherein the gate is driven into depletion while the substrate is simultaneously driven into accumulation.

15. The method of Claim 13, wherein capacitance-voltage measurements are taken to characterize the polysilicon gate depletion of the semiconductor device.

16. A method for forming a P-gate/P-substrate capacitor for characterizing polysilicon gate depletion effect corresponding to a semiconductor fabrication process, comprising the steps of:

forming a silicon substrate;

growing an oxide layer over the silicon substrate;

etching the oxide layer to define a first isolation oxide section and a second oxide section;

growing a gate oxide disposed between the first isolation oxide section and the second isolation section;

depositing a polysilicon gate layer over the gate oxide;

defining the polysilicon gate;

doping the substrate with P dopants;

doping the polysilicon gate with P+ dopants;

laying and defining a metal layer.

17. The method of Claim 16, wherein the gate is driven into depletion while the substrate is simultaneously driven into accumulation.

18. The method of Claim 16, wherein capacitance-voltage measurements are taken to characterize the polysilicon gate depletion of the semiconductor device.

19. A method of using an N-gate/N-substrate capacitor for characterizing polysilicon gate depletion corresponding to the steps of:

grounding an N doped substrate;

applying a voltage to an N+ doped gate comprised of a gate oxide layer disposed over the N doped substrate, a first isolation oxide disposed over the N doped substrate, and a second isolation oxide disposed over the N doped substrate;

varying the voltage applied to the N+ doped gate;

measuring a capacitance value corresponding to the N-gate/N-substrate capacitor as a function of the voltage being applied to the N+ doped gate;

determining the polysilicon gate depletion according to capacitance-voltage measurements.

20. A method of using an P-gate/P-substrate capacitor for characterizing polysilicon gate depletion corresponding to the steps of:

grounding a P doped substrate;

applying a voltage to a P+ doped gate comprised of a gate oxide layer disposed over the P doped substrate, a first isolation oxide disposed over the P doped substrate, and a second isolation oxide disposed over the P doped substrate;

varying the voltage applied to the P+ doped gate;

measuring a capacitance value corresponding to the P-gate/P-substrate capacitor as a function of the voltage being applied to the P+ doped gate;

determining the polysilicon gate depletion according to capacitance-voltage measurements.